EXPRESS MAIL LABEL NO.: EV343427443US
DATE MAILED: September 12, 2003 PATENT

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PROCESS FOR CONTACT OPENING DEFINITION FOR ACTIVE ELEMENT ELECTRICAL CONNECTIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims priority from prior European Patent Application No. 02-425558.0, filed September 12, 2002, the entire disclosure of which is herein incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the fabrication of integrated circuits, and more particularly to a process for contact opening definition for the active element electrical connections.

2. Description of Related Art

The active elements of an integrated circuit are connected to other elements through contacts. The number of contacts in a typical integrated circuit can vary from hundreds of thousands to about ten million.

The dimension reduction of integrated circuits leads to the realization of contacts having smaller and smaller dimensions, and thus requiring more and more precise and delicate fabrication processes. Further, the possible presence of extraneous substances in the processing environment can alter and contaminate a fabrication process in progress.

SUMMARY OF THE INVENTION

In view of these drawbacks, it is an object of the present invention to overcome these drawbacks and to provide an improved process for forming contacts in an integrated circuit.

Briefly, one embodiment of the present invention provides a method for contact opening definition for active element electrical connections. According to the method, a layer of BPSG is formed on a surface of an integrated circuit, and a transparent layer of nitride UV is formed above the layer of BPSG. Preferably, the transparent layer of nitride UV is formed by deposition using an HDP process and has a thickness of less than about 500Å.

Further embodiments of the present invention provide a machine-readable medium encoded with a program for contact opening definition for active element electrical connections.

Other objects, features, and advantages of the present invention will become apparent from the following detailed description. It should be understood, however, that the detailed description and specific examples, while indicating preferred embodiments of the present invention, are given by way of illustration only and various modifications may naturally be performed without deviating from the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1 to 4 show cross-sections of a conventional integrated circuit during fabrication; and

Figures 5 to 6 show cross-sections of an integrated circuit according to a preferred embodiment of the present invention during fabrication.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described in detail herein below with reference to the attached drawings.

The process for fabricating an integrated circuit is typically composed of the following steps:

1) growth of an active (tunnel) oxide 10;

2) deposition and definition of a polysilicon layer 11 that constitutes the floating gate (poly1) only in the active matrix and its elimination from the other circuitry;

3) deposition of an interpoly dielectric layer 12, for instance of the ONO (Oxide Nitride Oxide) type;

4) through a mask (MATRIX mask), the etching (generally dry) of the deposited layers of interpoly dielectric (for instance, ONO) and polysilicon (poly1) of the floating gate memory cells is effected;

5) growth of one or more layers of gate active oxide 13;

6) deposition of a second polysilicon layer 14 (poly2);

7) definition of the matrix cells through exposure of the auto-alignment mask; and

8) definition of the gates of the transistors through exposure of the circuit mask, formation of spacers 15 (for instance of oxide or nitride), and if necessary the formation of a metallic conductive layer 16 (for instance of titanium salicide, or cobalt or tungsten silicide).

Such steps lead to an integrated circuit as shown in the cross-sectional view of Figure 1. Subsequently the formation of the layers in which the contacts should be formed is effected through the following steps.

9) Deposition of an oxide layer of USG (Undoped Silicon Glass), for instance from an HDP (High Density Plasma) process and with a thickness in the range of about 500Å-2500Å, or of nitride (in which case a process known as "borderless" is used for the formation of the contacts), as shown in Figure 2. The presence of this layer prevents the spreading in the silicon and in the gates of contaminants derived from the doped layers that are subsequently deposited.

10) Deposition of a layer, for instance of BPSG (Boron Phosphorous Silicon Glass) (not necessary in circuits without non-volatile memories), generally through a

SACVD (Sub Atmospheric Chemical Vapor Deposition) process with concentration of the type 2:9 being useful, especially for memory flash devices, as shown in Figure 3.

11) Thermal treatment with RTA (Rapid Thermal Annealing) of the deposited BPSG layer.

12) Planarization of the premetal layer of USG and BPSG, for instance through CMP (Chemical Mechanical Polishing) technology.

At this point, according to the conventional process, the contact mask is exposed, which foresees two overlapped layers of BARC (Bottom Anti Reflecting Coating) and of resist, for the masks to be used in the exposure of the DUV (Deep Ultra Violet) type.

Such layers are necessary to allow the correct definition of the contacts according to the dimensional specifications required by the product. The presence of the BARC also avoids the contamination of the resist from the doped layer of BPSG, which if it happened would jeopardize the final result of the lithographic process.

Then, the selective removal of the BPSG and USG layers is effected through a dry etching of the oxide layers, generally using a chemistry of the $CHF_3/CF_4/O_2$ type, usually used for the oxide etching at the contact level. After the contact hole C is formed in the oxide layers (see Figure 4), it is filled with tungsten W through CVD deposition of the tungsten from WF_6 to form the tungsten W 'plug'. Generally, between the contact oxide and the tungsten W, a barrier layer of TiN (or Ti/TiN) is interposed from CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) to avoid contaminations of WF_6 and diffusion of the tungsten W through the oxide. Through dry etching (selective with the Ti/TiN layer, which is the end-point) there is removed (etched back) the tungsten W deposited in excess, so as to give definitive form to the contact. The operations for the deposition of the AlCu metal layers and the definition of the circuit interconnections follow.

According to the present invention, after step 12 of the conventional process described above, instead of immediately exposing the contact mask, a layer NIT, for instance of transparent UV (Ultra Violet) nitride, is deposited, preferably with a

thickness of less than about 500Å, and more preferably between about 100Å and 500Å, as shown in Figure 5. The layer NIT is preferably deposited through an HDP process, but any other process that is able to deposit a uniform layer at low temperature (for instance, < 500°C) can be utilized, for example a Chemical Vapor Deposition (CVD) process. The deposited layer NIT is preferably insulating in order to avoid any possible short circuit.

After that, two overlapped layers of BARC and of resist are formed, when necessary.

The deposited layer NIT must be made of a material that allows a high selectivity with the BPSG during the contact etching, so that once the resist is worn out (or has been consumed) it develops the same function of superior barrier layer (that is, above the BPSG layer) in comparison to the etching chemistry. For this purpose, it is advantageous that the deposited layer is for instance a transparent UV nitride that has high selectivity with the BPSG and does not prevent the reliable performance of the memory cell, particularly if the cell is of the flash type.

The function of such a layer is that of avoiding the direct contact of the BARC and resist with the BPSG, especially in case of prolonged rest of the wafers with BARC and resist already deposited and before their working (contact etching). In such a way, the defective formation called "corrosion" of the BPSG layer, which makes impossible the contact definition and therefore reduces yield, is avoided.

Additionally, such a layer avoids the formation of contacts "with double edge", which is critical when the contact dimension is on the order of 0.2μm or smaller and the distance between the contacts is on the order of 0.5μm.

Once the barrier layer has been deposited in accordance with the present invention, the normal operations of mask exposure of the contact and its etching are effectuated, as shown in Figure 6. Obviously the contact etching chemistry is modified in order to correctly etch the additional protective layer in the first step (being in this exemplary case a nitride layer, a dry etching of the protective layer having a chemistry of the type C_4F_8/O_2 can advantageously be used, to allow an elevated selectivity with the BPSG underlying oxide), and then proceeding in a

standard manner, for instance with a chemistry of the type CHF_3/O_2, to etch oxide once arrived at the BPSG.

The method of the present invention can be embedded in hardware, software, or a combination of hardware and software. Any processor, controller, or other apparatus adapted for carrying out the functionality described herein is suitable. A typical combination of hardware and software could include a general purpose processor (or a controller) with a computer program that, when loaded and executed, carries out the functionality described herein.

The present invention can also be embedded in a computer program product, which comprises all the features enabling the implementation of the methods described herein, and which - when loaded in an information processing system - is able to carry out these methods. Computer program means or computer program in the present context mean any expression, in any language, code or notation, of a set of instructions intended to cause a system having an information processing capability to perform a particular function either directly or after either or both of the following a) conversion to another language. Such a computer program can be stored on a computer or machine readable medium allowing data, instructions, messages or message packets, and other machine readable information to be read from the medium. The computer or machine readable medium may include non-volatile memory, such as ROM, Flash memory, Disk drive memory, CD-ROM, and other permanent storage. Additionally, a computer or machine readable medium may include, for example, volatile storage such as RAM, buffers, cache memory, and network circuits. Furthermore, the computer or machine readable medium may comprise computer or machine readable information in a transitory state medium such as a network link and/or a network interface, including a wired network or a wireless network, that allow a device to read such computer or machine readable information.

While there has been illustrated and described what are presently considered to be the preferred embodiments of the present invention, it will be understood by those skilled in the art that various other modifications may be made, and equivalents may be substituted, without departing from the true scope of the present invention.

Additionally, many modifications may be made to adapt a particular situation to the teachings of the present invention without departing from the central inventive concept described herein. Furthermore, an embodiment of the present invention may not include all of the features described above. Therefore, it is intended that the present invention not be limited to the particular embodiments disclosed, but that the invention include all embodiments falling within the scope of the appended claims.